Small-Signal and Temperature Noise Model for MOSFETs

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***Abstract*—The present CMOS technology provides n-channel MOSFETs with a transit frequency beyond 30 GHz, which are attractive for RF integrated circuits, e.g., low-noise amplifiers. This paper presents an improved deembedding procedure for extraction of parasitic elements of MOSFETs. The extraction determines the intrinsic elements of the small-signal equivalent circuit. As a result, a new method to determine the gate capacitance is presented. This deembedding procedure is based on an analytical solution of the equations and facilitates the determination of the elements at any specific frequency. Moreover, a temperature noise model is presented, which is based on the small-signal equivalent circuit with an analytical description of the channel noise. This enables a complete noise modeling of all four noise parameters and the determination of the dominant noise sources. Finally, the noise-figure measurements are compared with the simulation results.**

***Index Terms*—Deembedding, MOSFET, temperature noise model.**

I. Introduction

DECREASING channel length and consequently increasing transit frequency allow for the use of MOSFETs in RF-CMOS circuits and, thus, provide the fabrication of systems-on a chip. For circuit development, precise small-signal and noise equivalent circuits of the devices are required. Due to the resistive substrate losses of RF MOSFETs, a separation of interconnection network and intrinsic device is important (see Section II). Therefore, a two-step deembedding procedure is proposed to separate intrinsic transistor elements to obtain a valid transistor model for circuit simulation. Hereby, parasitic parallel elements introduced by the pads are first determined from an additional test structure, whereas series elements are then deduced from measurements at passive device biasing conditions. A new method for the determination of the channel resistance and gate capacitance is presented (i.e., cold modeling, seeSection III). The intrinsic elements can be obtained after separation of the parasitic elements (hot modeling, see Section IV).

A temperature noise model capable of predicting all four noise parameters at any frequency, any temperature, and operating point is presented (see Sections V and VI).

II. Small-Signal Equivalent Circuit

Fig. 1 shows the small-signal equivalent circuit of the MOSFET with common source configuration used for the deembedding procedure [1]. The intrinsic transistor is embedded by series resistors R_g, R_d, and R_s and series inductors L_g, L_d, and L_s representing the interconnection lines. In addition, the parasitics of the pad due to substrate losses are modeled by the capacitors $C_{\rm pg}$ and $C_{\rm pd}$ in series with the resistors $R_{\rm pg}$ and $R_{\rm pd}$. The small-signal equivalent circuit can be expanded with a substrate network if necessary. The two-step method separates these elements from the intrinsic device.

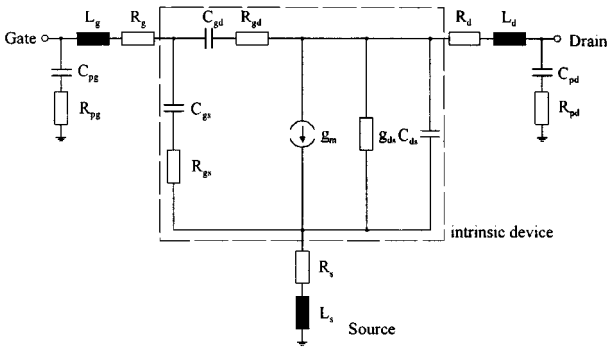

Fig. 1. Small-signal equivalent circuit of a MOSFET.

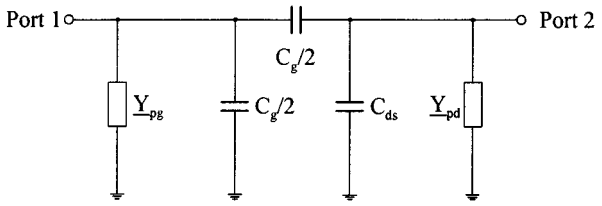

Fig. 2. Equivalent circuit of the MOSFET device for zero drain voltage and gate voltage below pinchoff.

III. Cold Modeling

First of all, the four elements, which are characterizing the pads ($C_{\rm pg}$, $C_{\rm pd}$, $R_{\rm pg}$, and $R_{\rm pd}$), are derived from a measurement of a test structure with the same metallization as the real structure, but without connected transistor (open structure) neglecting any coupling between gate and drain [2]. In the following, the gate and drain pads are represented by $\underline{Y}_{\rm pg}$ and $\underline{Y}_{\rm pd}$. The gate capacitance C_g is determined for the derivation of the still missing elements. Fig. 2 shows the valid small-signal equivalent circuit for a gate voltage below pinchoff and at zero drain voltage. In this case the transistor can be modeled by capacitors only. The circuit consists of the pads with $\underline{Y}_{\rm pg}$ and $\underline{Y}_{\rm pd}$, a gate capacitance subdivided to source and drain, a coupling capacitance between gate and drain, which is neglected

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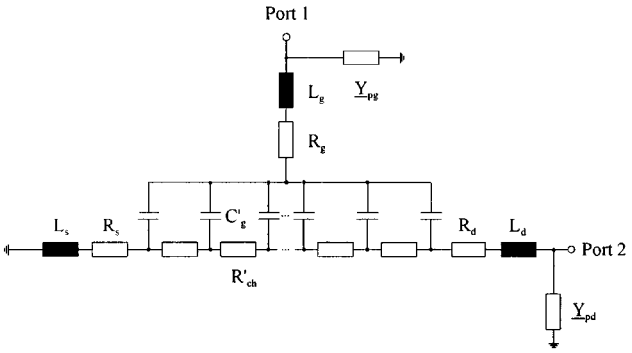

Fig. 3. Equivalent circuit of the MOSFET device for zero drain voltage and gate voltage above pinchoff.

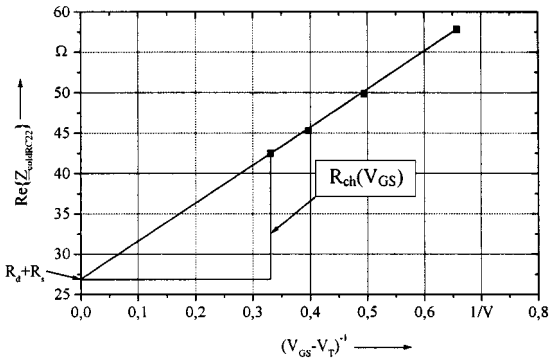

Fig. 4. Determination of the channel resistor $R_{\rm ch}$.

in the following, and a channel capacitance between source and drain.

The gate capacitance can be derived from the $\underline{Y}$-parameters of the small-signal equivalent circuit of Fig. 2 as follows:

$$C_g = \frac{2\left(\mathrm{Im}\left\{\underline{Y}_{11\mathrm{cold}C}\right\} + \mathrm{Im}\left\{\underline{Y}_{12\mathrm{cold}C}\right\} - \mathrm{Im}\left\{\underline{Y}_{\mathrm{pg}}\right\}\right)}{\omega}. \tag{1}$$

Fig. 3 shows the equivalent circuit, which is valid for a gate voltage above pinchoff and at zero drain voltage [3]. The intrinsic device is modeled through a distributed channel resistance $R'_{\rm ch}$ and a distributed gate capacitance C'_g.

The device is measured at different gate voltages for zero drain voltage. The channel resistance $R_{\rm ch}$ is determined from the real part of the $\underline{Z}_{22}$-parameter by extrapolating the sum of R_d and R_s at large gate voltages according to the following:

$$\mathrm{Re}\{\underline{Z}_{22}\} = R_d + R_s + R_{\rm ch} = R_d + R_s + \frac{1}{\beta}\frac{1}{(V_{\rm GS} - V_T)}. \tag{2}$$

Fig. 4 shows the determination of the channel resistance. The points in Fig. 4 are the measured values at different gate voltages and the line is the extrapolation, which allows the determination of the sum of R_d and R_s and thereby the calculation of the channel resistor $R_{\rm ch}$.

For the verification of the presented deembedding procedure, measurements were performed with a standard 0.35-μm CMOS process from the JESSI Project. The measurements were performed with a microwave probing system in the frequency range of 50 MHz–20 GHz. The method requires measurement results of an open structure and of an active device at different operating points for hot and cold modeling.

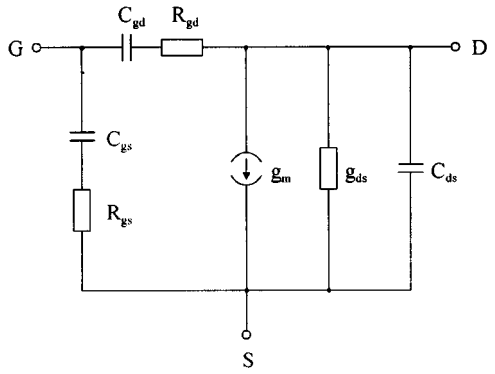

Fig. 5. High-frequency equivalent circuit of the intrinsic device.

The good agreement of measurement and interpolation justifies the equivalent circuit for zero drain voltage and gate voltage above pinchoff (Fig. 3).

With the knowledge of the gate capacitance C_g, channel resistance, and complete set of $\underline{Z}$-parameters for the equivalent circuit of Fig. 3, the remaining parasitic elements R_g, R_s, R_d, L_g, L_s, and L_d can be derived as follows:

$$\underline{Z}_{11} = R_g + R_s + \frac{R_{\rm ch}}{3} + j\left[\omega(L_g + L_s) - \frac{1}{\omega C_g}\right] \tag{3}$$

$$\underline{Z}_{12} = \underline{Z}_{21} = R_s + \frac{R_{\rm ch}}{2} + j\omega L_s \tag{4}$$

$$\underline{Z}_{22} = R_d + R_s + R_{\rm ch} + j\omega[L_d + L_s]. \tag{5}$$

The deembedding matrix for the series elements used in Fig. 1 is formulated as follows:

$$[\underline{Z}_s] = \begin{bmatrix} \underline{Z}_{11} - \dfrac{R_{\rm ch}}{3} + j\dfrac{1}{\omega C_g} & \underline{Z}_{12} - \dfrac{R_{\rm ch}}{2} \\ \underline{Z}_{21} - \dfrac{R_{\rm ch}}{2} & \underline{Z}_{22} - R_{\rm ch} \end{bmatrix}. \tag{6}$$

IV. Hot Modeling

Knowing all parasitic elements, the measured S-parameters can be deembedded from the parasitics, and the intrinsic Y_i-parameters can be deduced as follows:

$$[\underline{Y}_i] = \left[\left([\underline{Y}_a] - [\underline{Y}_{pad}]\right)^{-1} - [\underline{Z}_s]\right]^{-1}. \tag{7}$$

$\underline{Y}_i$ represent the $\underline{Y}$-parameters of the intrinsic device, which are calculated via matrix operations, where $\underline{Y}_a$ are the $\underline{Y}$-parameters of the measured device at the reference plane.

Fig. 5 shows the small-signal equivalent circuit of the intrinsic device with all parasitic elements subtracted. The

TABLE I
ELEMENT VALUES FOR AN OPERATION POINT IN SATURATION ($V_{DS} = V_{GS} = 2$ V) FOR A CHANNEL WIDTH OF $w = 43.75\ \mu$m AND A CHANNEL LENGTH OF $l = 0.35\ \mu$m

Element	Value
R_{pd}	0.8 Ω
R_{pg}	1.3 Ω
C_{pd}	110.4 fF
C_{pg}	114.1 fF
L_d	10.1 pH
L_g	26.7 pH
L_s	-18.5 pH
R_d	14.7 Ω
R_g	35.5 Ω
R_s	14.5 Ω
R_{gs}	11.1 Ω
C_{gs}	51.5 fF
C_{gd}	14.1 fF
C_{ds}	33.5 fF
g_{ds}	1.3 mS
g_m	10.3 mS
τ	679.3 fs

so-called "hot-modeling" allows the calculation of the elements by the $\underline{Y}$-parameters of the equivalent circuit as follows:

$$R_{gs} = \mathrm{Re}\left\{\frac{1}{\underline{Y}_{11}+\underline{Y}_{12}}\right\} \tag{8}$$

$$R_{gd} = -\mathrm{Re}\left\{\frac{1}{\underline{Y}_{12}}\right\} \tag{9}$$

$$C_{gs} = -\frac{1}{\omega}\frac{1}{\mathrm{Im}\left\{\dfrac{1}{\underline{Y}_{11}+\underline{Y}_{12}}\right\}} \tag{10}$$

$$C_{gd} = \frac{1}{\omega}\frac{1}{\mathrm{Im}\left\{\dfrac{1}{\underline{Y}_{12}}\right\}} \tag{11}$$

$$C_{ds} = \frac{1}{\omega}\mathrm{Im}\left\{\underline{Y}_{12}+\underline{Y}_{22}\right\} \tag{12}$$

$$g_{ds} = \mathrm{Re}\left\{\underline{Y}_{12}+\underline{Y}_{22}\right\} \tag{13}$$

$$g_m = \frac{|\underline{Y}_{12}-\underline{Y}_{21}|}{|\underline{Y}_{11}+\underline{Y}_{12}|\,\mathrm{Im}\left\{\dfrac{1}{|\underline{Y}_{11}+\underline{Y}_{12}|}\right\}} \tag{14}$$

$$\tau = -\frac{1}{\omega}\,\mathrm{arc}\left(\frac{j\,(\underline{Y}_{12}-\underline{Y}_{21})}{(\underline{Y}_{11}+\underline{Y}_{12})\,\mathrm{Im}\left\{\dfrac{1}{(\underline{Y}_{11}+\underline{Y}_{12})}\right\}}\right). \tag{15}$$

Table I shows the so-determined element values of an operating point in the saturation region for a device with a channel width of $w = 43.75\ \mu$m. The source inductance L_s is negative due to a numeric extraction accuracy problem, which can be solved using [4].

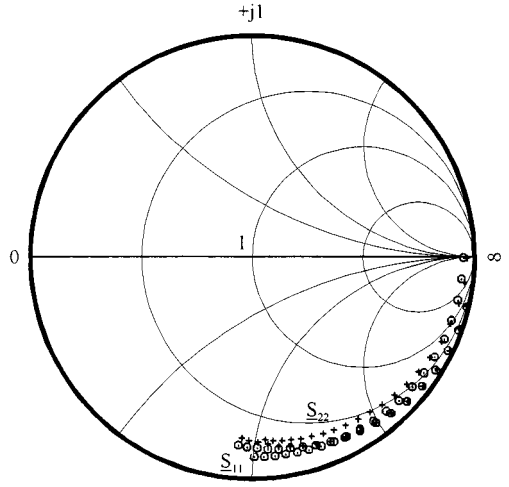

Fig. 6. Input and output reflection factors $\underline{S}_{11}$ and $\underline{S}_{22}$ of the intrinsic device in saturation (measurement: crosses, simulation: circles).

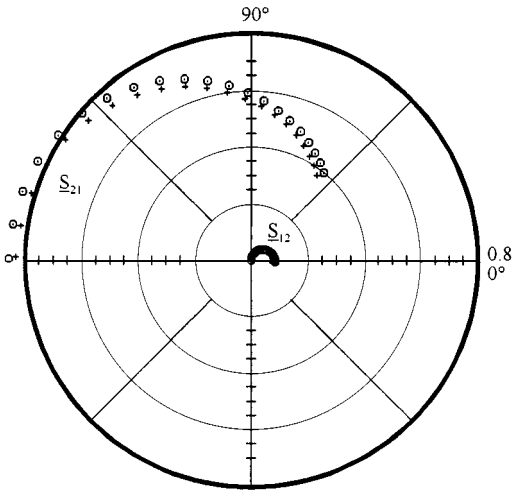

Fig. 7. Forward and reverse transmission factors $\underline{S}_{21}$ and $\underline{S}_{12}$ of the intrinsic device in saturation (measurement: crosses, simulation: circles).

Fig. 6 shows input and output reflection ($\underline{S}_{11}$ and $\underline{S}_{22}$) of the intrinsic deembedded device at saturation. Measured values are depicted as crosses and simulation results as circles.

$\underline{S}_{11}$ and $\underline{S}_{22}$ show good agreement with small deviations for high frequencies. In this case, the mean-square deviation is 1.9% for $\underline{S}_{11}$ and 4.5% for $\underline{S}_{22}$. Fig. 7 shows the transmission factors (forward and reverse) $\underline{S}_{21}$ and $\underline{S}_{12}$ of the intrinsic transistor in a polar plot.

Small deviations occur for $\underline{S}_{21}$ and $\underline{S}_{12}$ with a mean-square deviation of 1.3% for $\underline{S}_{21}$ and 10.2% for $\underline{S}_{12}$. To verify the validity of the equivalent circuits used at every step of the deembedding procedure, the frequency dependence of the elements has to be checked [5]. If there is no frequency dependence, the equivalent circuit is valid. As the deembedding procedure is frequency independent, the element values can be calculated at every frequency point. To illustrate this, Fig. 8 shows the frequency dependence of the capacitance C_{gd} in the frequency range of 0–20 GHz.

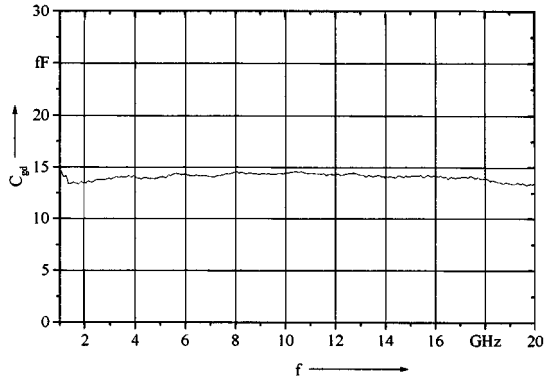

Fig. 8. Intrinsic capacitance $C_{\rm gd}$ versus the frequency.

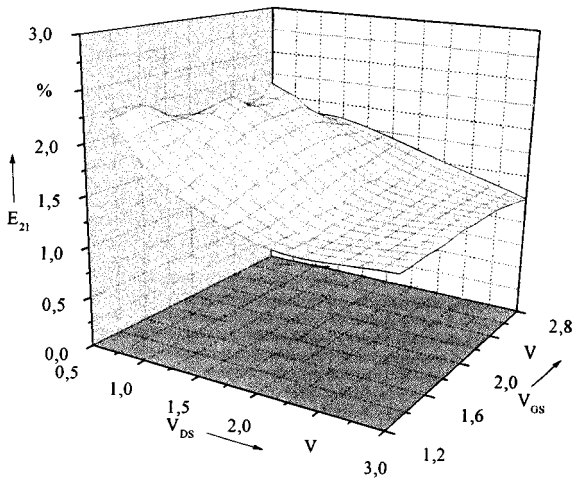

Fig. 9. Error term of the forward transmission factor E_{21} versus the operating point.

The extracted value of the intrinsic element $C_{\rm gd}$ shows almost no frequency dependence up to 20 GHz. Fig. 9 shows as an example the error term of the forward transmission factor E_{21} to demonstrate the independence of the extraction method for the operating point.

V. Noise Modeling

We propose a noise model based on the equivalent-circuit model of Fig. 1 including all intrinsic noise sources. In addition to the thermal noise of the resistors, the channel noise of the device is taken into account, which can be determined analytically or by a single measurement.

A. Small-Signal Equivalent Noise Circuit

We use a temperature noise model of the MOSFET for device characterization similar to [6]. The first step is the allocation of the intrinsic noise sources. In contrast to the already existing modeling approaches, the complete small-signal equivalent circuit of the MOS transistor, including all parasitic elements of the pads and interconnection lines, is used. Fig. 10 shows the proposed small-signal equivalent noise circuit of the MOSFET. The thermal noise of each resistor is described by the adequate noise current source. The noise generated by the channel current is modeled by the noise current source I_K.

B. Noise Sources

Typically, two noise sources are needed to characterize a noisy two-port [7]. As the small-signal equivalent circuit already describes the linear two-port characteristics, only the additional noise sources at the input and output are required to describe the four noise parameters of the device. As the gate is isolated from the channel, only thermal noise sources are considered at the input port. All resistors generate uncorrelated thermal noise according to their absolute temperature T_0, which is expressed through the effective value of the noise current i_R [see (16)] [8]

$$i_R^2 = \frac{4kT_0\Delta f}{R}. \tag{16}$$

k is the Boltzmann constant, T_0 is the ambient temperature, Δf is the frequency bandwith of interest, and R is any resistor of the equivalent circuit.

In addition to the thermal noise, we use only one noise source in parallel to the drain current source at the output. The diffusion noise is caused by the drain current and can be derived by an analytical equation (17), as described in [9]

$$\begin{aligned} i_K^2 = {} & 4kT_0\Delta f\mu_{\rm eff}^2 c_g^2 \frac{w^2}{l^2 I_D} \\ & \cdot \left[(V_{\rm GS}-V_T)^2 V_{\rm DSsat} - (V_{\rm GS}-V_T)V_{\rm DSsat}^2 + \frac{1}{3}V_{\rm DSsat}^3\right] \\ & - 4kT_0\Delta f \frac{wc_g\mu_{\rm eff}}{l^2 E_c}\left[(V_{\rm GS}-V_T)V_{\rm DSsat} - \frac{1}{2}V_{\rm DSsat}^2\right]. \end{aligned} \tag{17}$$

$\mu_{\rm eff}$ is the effective electron mobility, c_g is the gate capacitance per unit area, w is the channel width, l is the channel length, I_D is the drain current, $V_{\rm GS}$ is the gate-to-source voltage, V_T is the threshold voltage, $V_{\rm DSsat}$ is the drain-to-source voltage in saturation and E_c is the electric field at which electrons reach velocity saturation.

Equation (17) has to be replaced through (18) in case of an operating point in the triode region

$$\begin{aligned} i_K^2 = {} & 4kT_0\Delta f\mu_{\rm eff}^2 c_g^2 \frac{w^2}{l^2 I_D} \\ & \cdot \left[(V_{\rm GS}-V_T)^2 V_{\rm DS} - (V_{\rm GS}-V_T)V_{\rm DS}^2 + \frac{1}{3}V_{\rm DS}^3\right] \\ & - 4kT_0\Delta f \frac{wc_g\mu_{\rm eff}}{l^2 E_c}\left[(V_{\rm GS}-V_T)V_{\rm DS} - \frac{1}{2}V_{\rm DS}^2\right]. \end{aligned} \tag{18}$$

$V_{\rm DS}$ is the drain-to-source voltage.

On the other hand, the equivalent noise current I_K can be determined by a single noise measurement at any source impedance. As this is valid for each frequency, a verification of the model can also be done with measurements across a broad frequency range.

No additional correlation between the noise sources has to be calculated. The correlation is given through the transfer function of the device.

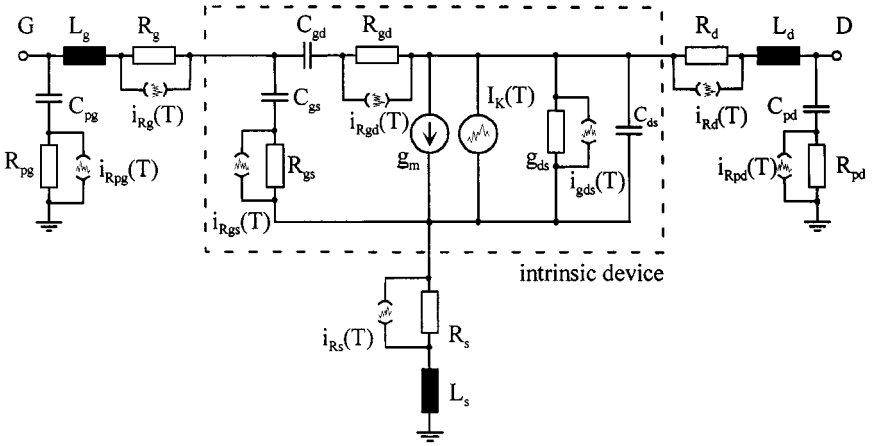

Fig. 10. Small-signal equivalent circuit of the MOSFET extended for noise modeling.

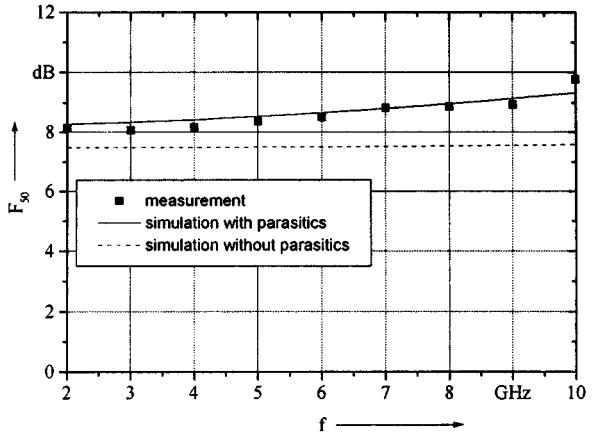

Fig. 11. Comparison of the measured noise figure of the MOSFET with simulation at a source impedance of 50 Ω.

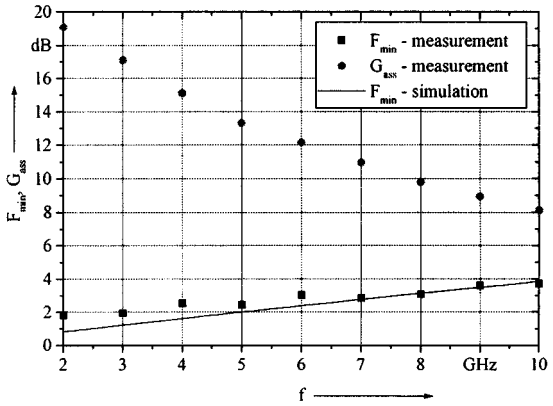

Fig. 12. Measurement of the associated gain (dots) and minimum noise figure (squares) of the MOSFET in comparison with noise model simulations.

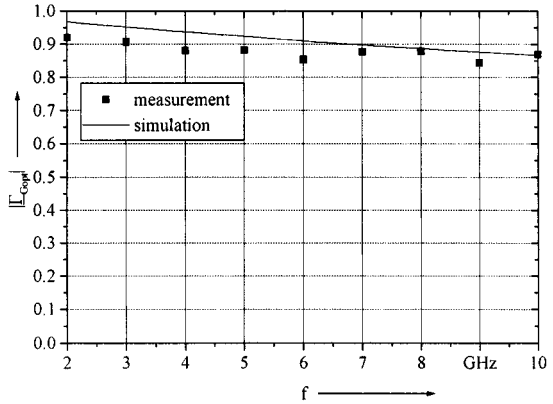

Fig. 13. Comparison of the measured absolute value of the optimum generator reflection factor of the MOSFET with simulation (measurement: squares).

VI. Noise Characterization

Fig. 11 shows simulation (performed with Agilent ADS) and measurement of the MOSFET's noise figure at a source impedance of 50 Ω, which can be easily performed in addition to S-parameter measurements.

Additionally, Fig. 11 shows the simulation of the device without pads and interconnection lines, resulting in a reduction of the noise figure of more than 1 dB.

The very large value of the noise figure is due to the source mismatch of the device. The minimum noise figure was measured additionally using an automatic tuned measurement system (Fig. 12). Due to a still mismatched source of the measurement system, there is a difference between measurement and simulation at very low noise figures. In addition, the experimental data of the associated gain are included, demonstrating the RF performance of the device. For comparison with measurements or other devices, the four noise parameters of a noisy two-port can be determined by simulation.

Fig. 13 shows the absolute value of the optimum generator reflection factor. This is the second noise parameter that can also be determined by a tuned noise measurement.

The large absolute value of the optimum generator reflection factor explains the great difference between the noise figure at 50 Ω and for minimum noise matching.

The comparison between measurement and simulation of the third noise parameter is shown in Fig. 14. It is the phase of the optimum generator reflection factor that can be modeled in good agreement to the measurements.

With the knowledge of the absolute value and the phase of the optimum generator reflection factor, the noise matching of the device can be achieved using standard circuit simulators.

The last noise parameter, i.e., the equivalent noise resistance, is shown in Fig. 15.

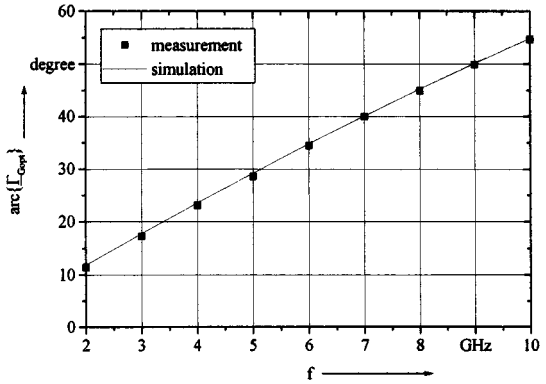

Fig. 14. Comparison of the measured phase of the optimum generator reflection factor of the MOSFET with simulation (measurement: squares).

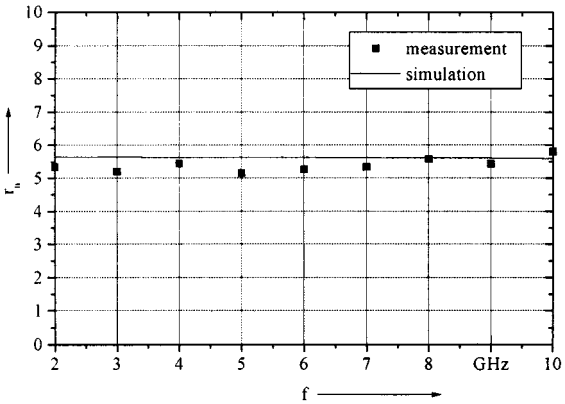

Fig. 15. Comparison of the measured equivalent noise resistance of the MOSFET with simulation (measurement: squares).

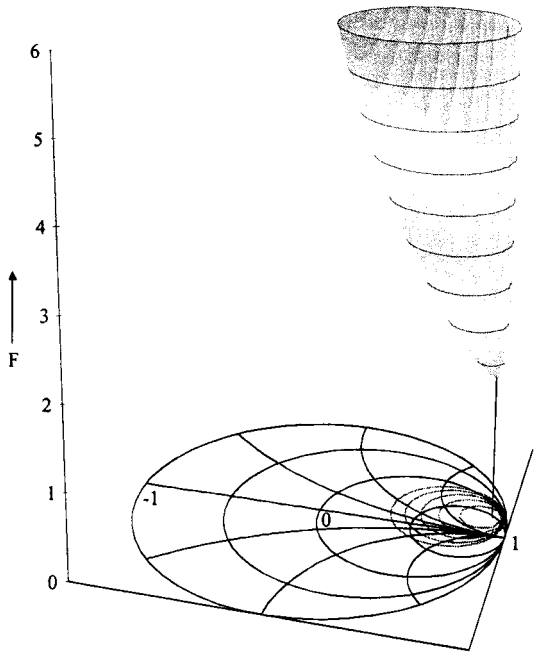

Fig. 16. Measurement of the noise paraboloid of the used MOSFET.

Fig. 16 shows the measured noise paraboloid of the MOSFET, which is determined by all four noise parameters.

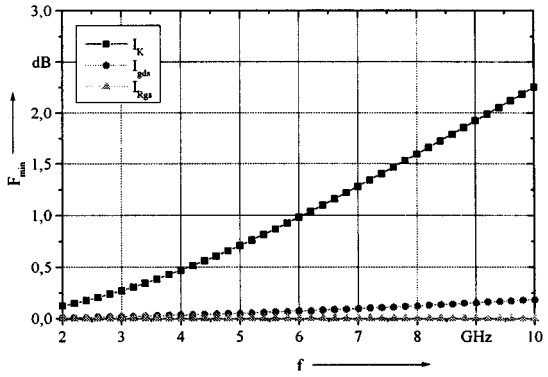

Fig. 17. Sensitivity analysis of the intrinsic noise sources at noise matching.

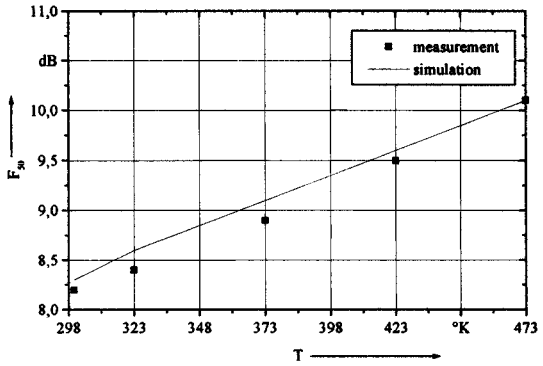

Fig. 18. Comparison of the measured noise figure (dots) with simulation (line) versus temperature ($V_{\rm GS} = V_{\rm DS} = 2$ V).

The very high equivalent noise resistance is responsible for the strong increase of the noise figure in case of a source mismatch. Therefore, the source matching is much more critical in MOSFET circuits. One key feature of the noise equivalent-circuit model is the ability to identify the noise contribution of each individual noise source for a given operating point at any frequency, as shown in the case of noise matching in Fig. 17. As expected, the channel noise is the dominant noise source for the MOSFET. The thermal noise of the resistors can be neglected in this frequency range.

A great advantage of the presented noise model is the ability to determine the noise parameters in dependence of temperature. As an example, Fig. 18 shows a comparison between measurement and simulation of the noise figure F_{50} at 50 Ω in dependence of temperature with good agreement.

A comparison of measurement and simulation of the minimum noise figure $F_{\rm min}$ can be used to show the independence of the operating point of the presented procedure. For this, Fig. 19 shows the measurement of the minimum noise figure $F_{\rm min}$ in regard to the operating point.

Fig. 20 shows a comparison of measurement and simulation of the minimum noise figure $F_{\rm min}$ at different drain–source–voltages $V_{\rm GS}$ with good agreement. The maximum deviation is less than 10% both in the triode and saturation regions.

The presented noise model can also be used to derive the absolute noise minimum of a device. Moreover, the noise figure can be extrapolated for higher frequencies. It requires in addition to the small-signal equivalent circuit only one parameter for

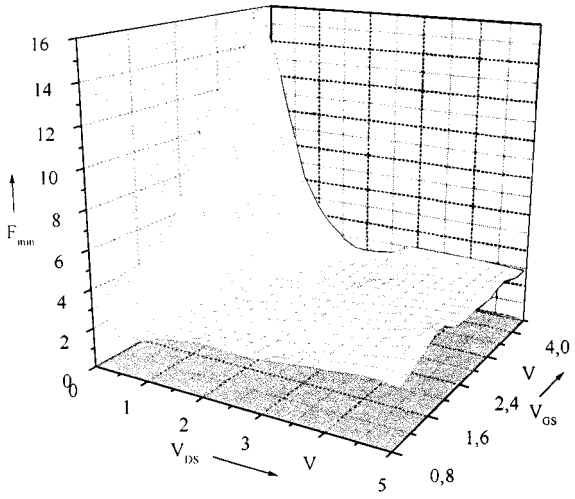

Fig. 19. Measured minimum noise figure versus operating point at a temperature of $T = 293$ K.

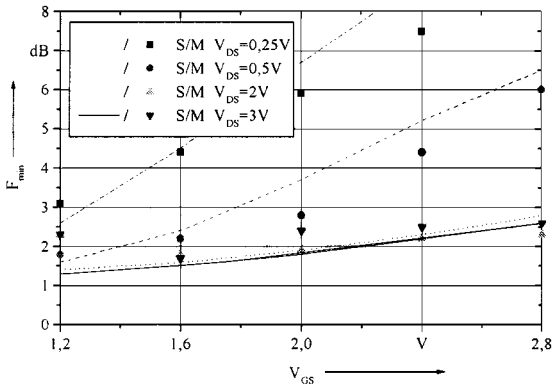

Fig. 20. Comparison of the measured minimum noise figure (dots) with simulation (lines) versus operating point at a temperature of $T = 393$ K.

the channel noise, which can be calculated or measured and can be used easily as a simulation model for computer-aided design (CAD).

VII. Conclusion

A new deembedding procedure for the derivation of the RF equivalent circuit has been described. As a result, a new method for the determination of the gate capacitance and channel resistance is presented. With the use of an open test structure and measurements at different bias conditions, parasitic elements can be determined using analytic equations. The analytic solution for parasitic and intrinsic elements allows the determination of the element values at any specific frequency. The validity of the small-signal equivalent circuits used for the procedure can be checked by examining the frequency dependence of the derived elements. This method allows quick derivation of the intrinsic small-signal equivalent elements for circuit development [10]. Moreover, a temperature noise model based on the small-signal equivalent circuit is presented. For the noise modeling, all intrinsic and parasitic noise contributions of the resistors are taken into account. The only additional noise source represents the channel noise and can be calculated analytically or measured at any frequency. The noise model can be used to determine the four noise parameters normally used for noise characterization in dependence of temperature, operating point, and frequency. With the knowledge of one noise measurement at a special frequency, even an extrapolation of the noise value versus frequency is possible.

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